TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT (Under 37 CFR 1.97(b) or 1.97(c))	Docket No. BOW5075.04A

In Re Application Of: **Robert W. Bower**

Serial No.	Filing Date	Examiner	Group Art Unit
10/033,715	12/28/2001	S. A. Gebremariam	8633

Title: **LIGHT EMISSION FROM SEMICONDUCTOR INTEGRATED CIRCUITS**

Address to:
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

37 CFR 1.97(b)

1. ☐ The Information Disclosure Statement submitted herewith is being filed within three months of the filing of a national application other than a continued prosecution application under 37 CFR 1.53(d); within three months of the date of entry of the national stage as set forth in 37 CFR 1.491 in an international application; before the mailing of a first Office Action on the merits, or before the mailing of a first Office Action after the filing of a request for continued examination under 37 CFR 1.114.

37 CFR 1.97(c)

2. ☒ The Information Disclosure Statement submitted herewith is being filed after the period specified in 37 CFR 1.97(b), provided that the Information Disclosure Statement is filed before the mailing date of a Final Action under 37 CFR 1.113, a Notice of Allowance under 37 CFR 1.311, or an Action that otherwise closes prosecution in the application, and is accompanied by one of:

   ☐ the statement specified in 37 CFR 1.97(e);

   OR

   ☒ the fee set forth in 37 CFR 1.17(p).

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LIGHT EMISSION FROM SEMICONDUCTOR INTEGRATED CIRCUITS

Payment of Fee

(Only complete if Applicant elects to pay the fee set forth in 37 CFR 1.17(p))

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

	Complete if Known
Application Number	10/033,715
Filing Date	12/28/2001
First Named Inventor	Robert W. Bower
Art Unit	8633
Examiner Name	S. A. Gebremariam
Attorney Docket Number	BOW5075.04A

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		Ellis, R. K. et al. "Electron Tunneling in Non-planar Floating Gate Memory Structure", IDEM, 1982, pp. 749-752.	
		Shealy, J.R. et al. "Direct band gap structures on nanometer-scale, micromachined silicon tips", Appl. Phys. Lett. Vol. 70, No. 25, June 1997, pp. 3458-3460.	
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		Dimitrijev, S. "Understanding Semiconductor Devices", Oxford Press, New York, ISBN 019513186X, 2000, Chapter 8, Photonic Devices, Fig. 8.10.	
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		Sze, S.M. "Physics of Semiconductor Devices", Wiley-Interscience, ISBN 0471056618, 1981, pp. 46, 47, 690, 691.	
		Wegener, H.A.R. et al. "The prediction of textured poly floating gate memory endurance", 23rd annual Proceedings on Reliability Physics, 1985, pp. 11-17.	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
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